REMARKS

In response to the non-final office action of October 19, 2005, applicants asks that all claims be allowed in view of the amendment to the claims and the following remarks.

Claims 11-12 and 14-31 are now pending, of which claims 11, 15, 18, 21 and 29 are independent and claims 23, 25, 27 and 28 have been withdrawn from consideration. Claims 29-31 have been added. No new matter has been introduced.

Rejection under 35 U.S.C. § 103

Claims 11, 12, 14-22, 24 and 26 have been rejected as being unpatentable over Sayyah (U.S. Patent No. 6,589,811) in view of Ding (U.S. Patent No. 6, 737,300). Applicant requests reconsideration and withdrawal of this rejection because neither Sayyah, Ding, nor any proper combination of the two, describes or suggests dividing the element layer into at least one integrated circuit film, as recited in each of independent claims 11, 15, 18 and 21, and for the additional reasons set forth below.

Claim 11 recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over a first substrate. The method also includes forming an element layer that includes an element using the crystalline semiconductor film, a wiring for transmitting an electrical signal to the element, and an insulating film. The method further includes transferring the element layer from the first substrate to a second substrate, transferring the element layer to a sheet, and dividing the element layer into at least one integrated circuit film.

The rejection indicates that Sayyah discloses, in Figs. 3a-3f and related text, a method of forming a semiconductor device including forming an element (1) in a film (2) on a first substrate (5), transferring the element layer to a second substrate (20), and transferring the element layer to a sheet (12). The rejection appears to rely on Ding's disclosure of cutting an individual chip scale package 100 from an assembly of multiple such chip scale packages for showing the step of dividing the element layer into at least one integrated circuit film, as recited in each of the independent claims. See Ding at FIGS. 13-14; col. 3, lines 1-37; and col. 4, line 66 to col. 5, line 5. Ding's individual chip scale package 100 includes a substrate attached to the active surface of a semiconductor chip 130 through an anisotropic conductive adhesive film 120 and multiple contact pads 110a provided with the lower surface of the substrate 110.

However, Ding's disclosure of cutting an individual chip scale package cannot be properly combined with Sayyah's method of forming a semiconductor device. One skilled in the art would not have been motivated to combine the cutting method of Ding with Sayyah's method of forming a semiconductor device. Nothing in Ding or Sayyah would have provided motivation to incorporate Ding's cutting of individual chip scale packages with Sayyah's method of forming a semiconductor device. Contrary to assertions made in the rejection, allowing for a more reliable electrical connection between structures is not sufficient motivation for combining Ding with Sayyah. Nor does the mere existence of a cutting method provide motivation to incorporate Ding's cutting of chip scale packages with Sayyah's method of forming a semiconductor device.

Moreover, while Ding describes cutting of individual chip scale packages, an individual chip scale package is not an integrated circuit film. As evidence of this, the specification points to the difference: "An integrated circuit film formed by a technique for transferring is a film including a semiconductor layer with a thickness of from 30 nm to 60 nm, and is much thinner than a semiconductor chip." See specification at page 3, lines 4-6.

As such, Ding does not remedy Sayyah's failure to describe or suggest dividing the element layer into at least one integrated circuit film, as recited in independent claim 11.

In addition, Sayyah's film (2) (referred to as a sheet transfer layer 2) is not disclosed to be a crystalline semiconductor film, as recited by claim 11.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 11 and its dependent claims 12 and 14.

Claim 15 also recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over a first substrate and dividing the element layer into at least one integrated circuit film. The method of claim 15 also includes forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring; transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer; forming a thermal conductivity film on the element layer; and transferring the element layer and the thermal conductivity film from the second substrate to a sheet.

The rejection relies on Ding for disclosing that protrusions can be formed on an element and can be used with a conductive adhesive to electrically bond the elements to a structure (citing FIGS. 13-14 and related text). However, the rejection provides no indication of where a

thermal conductivity film is disclosed in Sayyah or Ding. Moreover, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests transferring the element layer and the thermal conductivity film from the second substrate to a sheet, as recited in claim 15.

In addition, as described above with respect to claim 11, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests dividing the element layer into at least one integrated circuit film or forming a crystalline semiconductor film over a first substrate, as also recited in claim 15.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 15 and its dependent claims 16 and 17.

Claim 18 recites a method for manufacturing a semiconductor device that includes forming an element layer that includes a thin film transistor having a semiconductor layer including at least a channel forming region, a wiring connected to the thin film transistor, and an insulating film over a first substrate. The method also includes forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring; transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer; forming a thermal conductivity film on the element layer; and transferring the element layer and the thermal conductivity film from the second substrate to a sheet. The method further includes dividing the element layer into at least one integrated circuit film.

As described above with respect to claims 11 and 15, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests dividing the element layer into at least one integrated circuit film, or transferring the element layer and the thermal conductivity film from the second substrate to a sheet, as recited in claim 18.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 18 and its dependent claims 19 and 20.

Claim 21 recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over a first substrate and forming an element layer that includes an element using the crystalline semiconductor film, a wiring for transmitting an electrical signal to the element, and an insulating film. The method also includes forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring; transferring the element layer from the first substrate to a second substrate so as to dispose the

protruding electrode between the second substrate and the element layer; forming a thermal conductivity film on the element layer; and transferring the element layer and the thermal conductivity film from the second substrate to a sheet. The method further includes dividing the element layer into at least one integrated circuit film. The method also includes electrically connecting the integrated circuit film to an electrode of a wiring board by the protruding electrode, and removing the sheet from the integrated circuit film.

As discussed above, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests transferring the element layer and the thermal conductivity film from the second substrate to a sheet, dividing the element layer into at least one integrated circuit film, or using a crystalline semiconductor film. Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 21 and its dependent claims 22, 24 and 26.

In addition, each of claims 14, 17, 20 and 22 recites forming a film having a thermal conductivity of 10 W/m · K or more over the element layer after transferring the element layer to the second substrate. However, the rejection provides no indication as to where such a thermal conductivity film is believed to be disclosed in Sayyah or Ding, and applicant has found no such disclosure. Accordingly, for this additional reason, applicant requests reconsideration and withdrawal of the rejection of claims 14, 17, 20 and 22.

Further, claims 12, 16 and 19 each recite that the protruding electrode is formed before transferring the element layer to the second substrate. While Ding discloses a protusion, Ding does not describe or suggest transferring the element layer to a second substrate, nor does the rejection contend that Ding does so. As such, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests forming the protruding electrode before transferring the element layer to the second substrate.

Therefore, for this additional reason, applicant requests reconsideration and withdrawal of the rejection of claims 12, 16 and 19.

New Claims 29-31

Claim 29 recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over an insulating substrate and forming an element layer that includes an element using the crystalline semiconductor film, a wiring for transmitting

an electrical signal to the element, and an insulating film. The method also includes transferring the element layer from the insulating substrate to a substrate, transferring the element layer to a sheet, and dividing the element layer into at least one integrated circuit film.

As described above, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests dividing the element layer into at least one integrated circuit film or a crystalline semiconductor film, as recited in claim 29. Accordingly, for at least these reasons, applicant submits that claim 29 and its dependent claims 30 and 31 are allowable.

Conclusion

Applicant submits that all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a check in the amount of $300.00 for excess claim fees. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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